CLAIMS

What is claimed is:

1. An integrated circuit device (110) comprising: an integrated circuit (130) having a plurality of grounding pads, signal pads, and power pads; and a package (110) for mounting the integrated circuit and including a conductive path (140) having at least one reference trace surrounding the integrated circuit and having a grounding arch (170), disposed over the integrated circuit (130).

2. The integrated circuit device of claim 1 wherein the reference trace is coupled to at least one of the following: a voltage reference, a ground reference.

3. The integrated circuit device of claim 1 wherein, the grounding arch has an area comparable to the area of the integrated circuit device.

4. The integrated circuit device of claim 1 wherein the grounding arch is comprised of metal tape (160) laminated with a dielectric material (145).

5. The integrated circuit device of claim 4, wherein the grounding arch has a predetermined thickness thereby providing sufficient structure preventing electrical contact between the grounding arch and wire bonds.

6. The integrated circuit device of claim 1 wherein the grounding arch is coupled to at least one grounding location on the integrated circuit device, wherein the grounding location includes, the grounding trace (250a, 250c) and grounding pads (225).

7. The integrated circuit device of claim 6 wherein the grounding location furthers includes a location about a center region (250b) on the integrated circuit device.

8. The integrated circuit device of claim 5 wherein the grounding arch comprises conductors of a highly conductive material selected from: copper, gold, silver, aluminum and an alloys thereof.

9. The integrated circuit device of claim 5 wherein the highly conductive material is in a form including solid tape, mesh, and woven wire bonds.

10. The integrated circuit device of claim1 wherein the grounding arch is coupled to the grounding location with at least one of the following: conductive glue, solder, eutectic metal bond, a thermo-compression bond.

11. The integrated circuit device of claim 3, wherein the dielectric material is selected from at least one of the following: epoxy, polyimide, polyamide, solder mask, PTFE, and TEFLON™.

12. A method (600) for controlling impedance of bond wires in packaging a semiconductor device die in a package, the method comprising: defining locations (605) of signal and power/ground pads on the device die; defining grounding trace (605) locations on the package; bonding the signal pads and power/ground pads (610) of the device die; providing a conductive path including a ground arch over the bond wires and grounding trace locations (615, 620); and encapsulating the device die and ground arch (625).

13. The method of claim 12 wherein providing a conductive path further includes, rotating the package a pre-determined amount; and providing an additional ground arch.

14. The method of claim 13 wherein the pre-determined amount is about 90o.

15. The method of claim 13, wherein providing an additional ground arch is a function of device design, package size, number of wire bonds, and a desired impedance.

16. The method of claim 15, wherein the desired impedance is function of a ground arch distance from a wire bond.